Daniel Besse | Digital IC Design Engineer

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ASIC design engineer with 10+ years of experience and 20+ tapeouts.

I am a dedicated engineer with wide experience in ASIC design and the whole RTL-to-GDSII plus verification flow. In small teams, I have taken responsibility for the design, verification, and backend of complex digital systems, contributing to over 20 tapeouts across a wide range of technology nodes.

Work Experience

CSEM AG — Zürich
Senior IC Designer (80%), Low-power SoC design. — *Apr 2024 – current*

RISC-V SoC SystemVerilog implementation of Ibex-based RISC-V systems and custom hardware accelerators for cryptography (AES, ECC, PQC).

Edge AI / NPU Custom Neural Processing Unit (NPU) accelerator design and development of an ONNX compiler toolchain in Python.

Verification Functional verification using UVM and SystemVerilog Assertions (SVA).

Low-Power Architecture and implementation featuring multiple power domains, clock domain crossing (CDC) analysis, and linting.

Backend Physical RTL-to-GDSII flow and DFT using Cadence digital suite (Genus, Innovus, Modus) across technology nodes from 180 nm down to 22 nm. Contributing to about 4 tapeouts per year.

AlpsenTek GmbH — Zürich
Senior IC Design Engineer (80%), Hybrid biomimetic vision sensors. — *Aug 2021 – Nov 2023*

RTL SystemVerilog implementation of active pixel sensor (APS) data readout and analog pixel array driving. APB bus structure for configuration register banks and I2C control interface.

IP-XACT Complete rework of register banks to conform to IP-XACT with auto-generation of SystemVerilog, documentation, C-header files, and UVM register abstraction layer (RAL) database.

Git CI Deployment of GitLab Continuous Integration pipelines for quality assurance, running lint checks as well as regression test suite. Build management and git repositories setup for digital IP reuse.

ACP Advanced Circuit Pursuit AG — Zürich
Design Engineer (90-100%), Multi-mode RFIC and SoC devices. — *Mar 2016 – Jul 2021*

DSP model MATLAB modeling of transmitter (Rx and Tx) signal processing algorithm. Use of cycle-exact models as golden reference for hardware design.

RTL VHDL implementation of digital signal processing (DSP) algorithms, specific modules for 3GPP wireless protocols, as well as SerDes interfaces for data and control (RBDP/DigRFv4/JESD204/SPI/...).

RISC-V SoC Architecture for system-on-chip in 22 nm including several power domains, a LowRISC ibex core, and legacy signal processing blocks from externally-controlled device in 130 nm.

Backend Physical RTL-to-GDSII flow using Cadence digital suite in both 130 nm and 22 nm.

Firmware Embedded-C code for multi-stack firmware targeting the internet-of-things (IoT) and running on the RISC-V core of our own SoC. Real-time stack arbitration and layer 1 for GSM fallback.

Texas Instruments — Freising (D)
Intern (100%), Automated MCU digital power simulations for the MSP430. — *May – Oct 2013*

Power Firmware testcases and power simulations for MSP430 microcontroller.

Education

École Polytechnique Fédérale de Lausanne (EPFL) — Lausanne
Bachelor and Master, Electrical Engineering — *2010 – 2016*

Master **Best EE GPA**. Gilbert Hausmann Award. Excellence scholarship. **GPA 5.83/6.00**.
Master thesis: semi-custom digital flow with custom-made 28 nm FD-SOI standard cells for 50 GS/s digital down converter.
Semester project: inexact adder architectures and optimization of the accuracy-resource tradeoff for audio codec applications.

Bachelor **Best EPFL GPA award** (out of 1800+ students). **GPA 5.91/6.00**.
Internship: 13-bit AD/DA converter design using Cadence Virtuoso in a mixed-signal project.

Georgia Institute of Technology Atlanta (USA)
Bachelor, Electrical and Computer Engineering *2012 – 2013*

Exchange Senior year (bachelor) as an exchange. **GPA 4.0/4.0**.

Languages

Native: French
Fluent: English, German
Basic: Italian

Skills

Experienced: Cadence Digital Suite (Genus, Innovus, Modus DFT), SystemVerilog, VHDL, UVM, Python, Git
Advanced: SVA, Multi power-domains, CDC, Linting, C, Tcl, Bash/Unix, GitHub Copilot
Basic: C++, Verilog, MATLAB, Cadence Virtuoso

Interests

Sport: Triathlon at national and international level for more than 15 years.
Projects: Small electronics projects, VR film production, and full-stack web development.